High Power Components

From the State of the Art to Future Trends

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Abstract

This paper addresses the current state and trends of bipolar and BIMOS high power devices and their packages.

At the highest power and voltage levels the GCT/IGCT is consolidating its position and is gradually substituting the GTO. The maximum GCT ratings in terms of current and voltage are more determined by market forces than by device physics.

Improved plasma engineering in high voltage IGBT's will lead to further reduction of losses. The major tools for plasma engineering are discussed.

Modern simulation tools allow to determine the performance limits of a Si diode at a given voltage. Today's best diodes are not very far from this limit. The diode is a performance limiting element in many high voltage circuits. Recent progress in SiC technology makes hybrid solutions consisting of Si switches and SiC diodes feasible.

Module packages for traction applications still need some derating due to extreme power cycling reliability requirements. Better thermomechanical matching has lead to major improvements. The antagonism between standardization and integration is hotly debated.

1. Introduction and Overview

The field of high power semiconductor devices is relatively mature but still evolving at remarkable speed. This means that the rate of innovation is high but also reasonably predictable. Tab. 1 gives the major drivers for innovation.

	Low Voltage AC Drives	**Locomotive Drives**	**Transmission & Distribution**
First Choice	low cost	reliability (wear-out & FIT)	reliability (redundancy) series-connection
Second Choice	reliability (FIT)	low cost	low losses
Choice Drivers	low component-count, standardization	low component-count	low component-count,

Tab.1 Innovation drivers in power electronics systems and circuits

As far as switches are concerned, the IGBT at voltages up to 3.3 kV and the GCT at 4.5 kV and higher seem to be the winners. With the remarkable progress of both IGBT and GCT towards the "ideal switch" the quest for the "ideal diode" becomes more and more prominent. This is particularly true for snubberless operation in which the IGBT has to be slowed down to guarantee survival of the freewheel diode.

Classical press pack devices had a clearly defined interface to the rest of the circuit. Multichip packages offer much more degrees of freedom. Innovative packaging solutions provide substantial reduction in cost, volume and parts count if they are the result of an overall system optimization.

The cost of a high power device can be split into the cost of the die-free package and silicon cost. The package cost is mostly material cost, whereas the silicon cost scales with yield and area. In GTO's the silicon area is usually determined by the turn-off limit. For GCT's and IGBT's, thermal criteria and for IGBT's in traction applications also wear-out criteria prevail. This defines the major innovation routes: Decrease material cost by modularization and standardization, decrease silicon cost by loss reduction and by improved thermal management.

Reliability is another parameter high on the priority list. Early failures can be further reduced by a strict application of the 6 σ concept in the whole chain from the raw material supplier to the system manufacturer. Assuming properly designed components, the FIT rate (flat portion of the curve in Fig. 1) scales mostly with system complexity. Reducing parts count and integration are the major tools to reach state of the art FIT values. A failure rate of 100 FIT (1 failure per 10^7 element hours) or better is required.

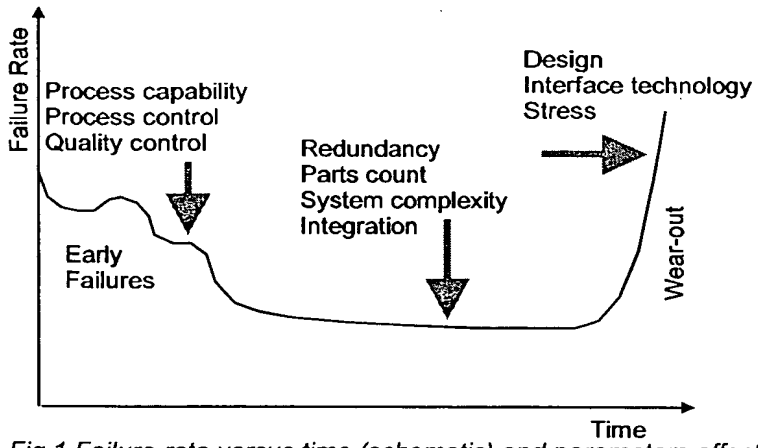

Fig.1 Failure rate versus time (schematic) and parameters affecting the various regions.

In particular for traction applications wear-out is a major concern as evident from Tab. 2. Wearout problems can always be solved by overdesign, which implies higher cost. Further improvements will make larger thermal amplitudes and thus lower cost possible. Fig. 1 gives a schematic failure rate curve and identifies the parameters which control the different parts.

Stress cycle	stop to stop	station to station	day to day	year to year
Train system	ΔT_j/# of cycles	ΔT_j/# of cycles	ΔT_j/# of cycles	ΔT_j/# of cycles
Metro/Tram/Bus	$40K/10^7$	$50K/10^6$	$60K/10^4$	170K/30
Suburban	$50K/2*10^6$	$60K/10^5$	$80K/10^4$	170K/30
Intercity/High speed Trains	$60K/2*10^5$	$80K/4*10^4$	$100K/10^4$	170K/30

Tab. 2 Worst case temperature swings for IGBT modules in traction applications [1].

2. Bipolar Devices

The high power thyristor technology is very mature and no major innovation steps are on the horizon. ABB is now introducing its BCT (Bidirectional Control Thyristor) generation. The BCT [2] consists of two antiparallel thyristors on one wafer with two independent gates. This leads to substantial savings in clamping and infrastructure and allows more compact designs.

For blocking voltages below 4.5 kV the GTO is more and more substituted by IGBT solutions. At voltages of 4.5 kV and higher the GCT and IGCT (Integrated Gate-Commutated Thyristor) is expected to replace the GTO. The GCT consists of a low loss, n-buffer GTO structure in a specially designed low inductance housing [3]. The key is that at turn-off the load current is commutated to the gate in about 1 µsec such that the cathode junction is depleted before the main junction takes on voltage. This sup-

presses the regenerative process which is the cause for the notorious turn-off instabilities of the GTO. The device can thus be turned off without any dV/dt snubber. Snubberless turn-off is limited in most cases by the gate unit which has to be able to supply the full load current within 1 µsec. With appropriate gate units a maximum turn-off power of 500 kW/cm^2 has been realized. ABB's GTO structure [4] has a buffer layer to reduce device thickness and thus losses and a homogeneous, low efficiency anode to minimize trigger and back-porch currents (Fig.2).

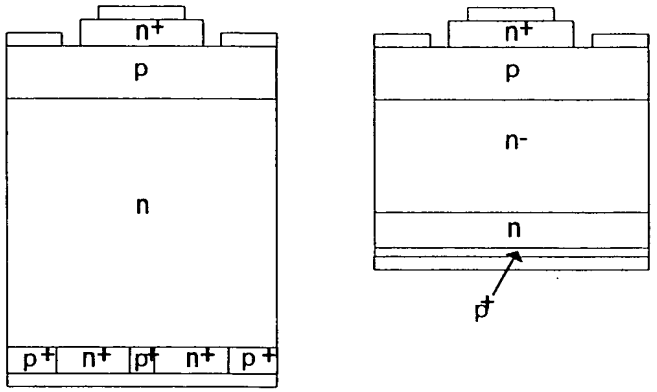

Fig. 2 Standard GTO structure (left) with anode shorts, TGTO with n buffer and homogeneous, low efficiency anode (right)

The aggressive reduction of stray inductance makes it possible to achieve slopes of more than 3 kA/µsec with a gate voltage below the gate - cathode breakdown voltage of the GTO. This reduces commutation of the load current merely to the discharge of a low-voltage capacitor (Fig. 3).

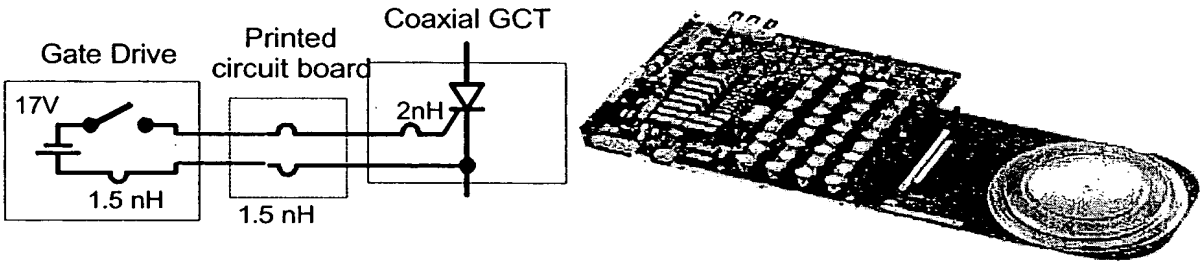

Fig. 3 4 kA IGCT with 5 nH total stray inductance.

GCT's and IGCT's of 4.5 kV and 6 kV blocking voltage are now available in different current ratings from more than one supplier. 6 kV types are used in a new medium voltage drive generation of ABB Industry. GCT's have proven their superiority to GTO's in series connection applications such as interties.

Assuming a limit of 500 kW/cm^2 for turn-off SOA and a device area of 60 cm^2 (a typical area of a 3 kA GTO) results in a turn-off limit at 3 kV of 10 kA for snubberless operation! This, however, would require a gate unit which provides 10 kA/µsec. Operation at < 20 V restricts the total stray inductance to < 2 nH. This has not been achieved, but 6 kA turn off of a 60 cm^2 device has been demonstrated.

The hard drive reduces the storage time to about 1 µsec. This removes the obstacles for series connection without complex and costly control systems which constantly monitor and compensate the jitter in storage time.

3 kA, 4.5 kV, 125°C unless otherwise stated	GTO standard (anode shorted)	GCT standard (HD-GTO)	TGTO	GCT (n-buffer, T-anode)
	91 mm devices			
on-state voltage V_{tm}	3.8 V	3.8 V	2.2 V	2.2 V
turn-off energy E_{off}	10 Ws at 4 µF	13 Ws at 0 µF	9 Ws at 4 µF	14 Ws at 0 µF
turn-on energy E_{on}	5 Ws at 500 A/µs	1 Ws at 3000 A/µs	0.2 Ws at 500 A/µs	1 Ws at 3000 A/µs
snubber requirements C_s	3 to 6 µF	0 to 3 µF	3 to 6 µF	0 to 3 µF
rms current I_{rms}, at Tc = 85°C	1570 A	1570 A	2200 A	2200 A
on-state loss at 1 kA dc	2900 W	2900 W	1450 W	1450 W
peak turn-off current I_{tgq}	4 k A	3 to 6 kA	3 kA	3 to 6 kA
gate drive power at f_t = 500 Hz, 1150 A_{RMS} (3)	80 W	35 W	30 W	30 W
max. turn-off dv/dt	1000 V/µs (1)	3500 V/µs (2)	1000 V/µs (1)	3000 V/µs (2)
I_{gt} at 25 °C	4 A	4 A	0.4 A	0.4 A
typical back-porch at -40 °C	18 A	18 A	2 A	2 A
thermal resistance $R_{th\text{-}jc}$	0.011 °C/W	0.011 °C/W	0.011 °C/W	0.011 °C/W

Tab. 2 Comparison of the standard GTO, hard driven standard GTO (GCT), TGTO (standard drive) and state of the art GCT. (1) rating, (2) characteristic.

GTO and GCT operation at high dc link voltages (> 3 kV) and high junction temperatures has been limited by passivation stability. Electroactive passivations (a-C:H) [5] will substantially increases the temperature range. 9 kV GCT's seem feasible and their successful development will start as soon as a market demand has been identified. For a high voltage, medium current IGCT, the demands on the stray inductance of the system and gate unit power are very modest. The IGCT is thus an ideal element for such applications.

By introducing a buffer layer, the optimum axial doping profiles for a GTO and for a fast recovery diode become virtually equal. This allows the monolithic integration of the freewheeling diode without compromising performance. In older designs the diode had substantial performance degradation. Integration of the freewheeling diode leads to reduction in cost and parts count.

Traditionally diodes (snubber and freewheel) in GTO circuits have been operated at a few 100 A/µsec. The important device parameters were conduction and switching losses. With GCT's, slopes of 1000 A/µsec and more are required and also achieved. Diode SOA (Safe Operating Area) becomes then a highly relevant parameter [6]. This is qualitatively new.

The use of electroactive passivation will reduce the need for a hermetic package. Low cost non-hermetic packages without reduction of reliability and environmental stability become feasible.

3. Module Packages

There are two main drivers in the further evolution of module packages. The first is reliability increase, the second is cost reduction. Both are intimately related but to some extent antagonistic.

In order to bring some structure into the discussion, we first discuss a few generic questions. Most modules today have the chips soldered on the anode side and wire bonded on the cathode side. Another category which we will call Press Pack has at least one dry interface which is pressure contacted. Press Pack modules have been developed e.g. by Fuji, Toshiba and ABB. The original motivation in most cases was the poor power cycling capability of early versions of wire bonded modules and their explosion behavior.

There is, however, a second reason to use Press Pack modules. In a properly designed Press Pack the failure mode is well defined and consists of a stable short circuit. The failure mode of a wire bonded package is poorly defined but most likely ends up in open circuit. Open circuit is the desired failure mode for parallel connection because it allows for redundancy.

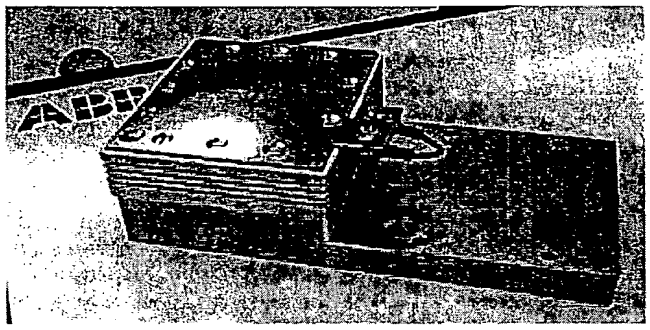

Fig. 3 Press Pack module (2.5 kV, 700 A) for series connection

The opposite is true for series connection. For high voltage applications in power transmission and distribution the series connection of a large number of devices is mandatory. If in a redundant stack of devices a failure occurs and if the failed devices becomes short circuit, then the stack will remain functional. A wire bonded module in series connection has an ill defined failure mode. This rules it out for applications in power distribution and transmission where a redundant series connection is mandatory.

The question of integration is widely discussed. At smaller power levels where integration of the whole converter is feasible, integration is clearly a goal and will lead to cost savings. At high power levels only partial integration is possible. Halfway integration always implies loss of flexibility. In the resulting integration vs. modularity dilemma, the market seems to go in the direction of modularity. High volume, standard purpose modules offer an economy of scale which is very hard to beat by integrated solutions of smaller market volume. It is fair to state, however, that this is hotly debated and that there are different views on this subject.

Another generic issue to be addressed is the explosion hazard of wire bonded modules. Modern IGBT converters have a low stray inductance and no reactive dI/dt limitation. If a failure occurs, then the stored energy of the capacitor bank will be instantaneously released. The wire bonds vaporize and most of the energy is dumped in plasma energy. If the plasma is constricted into a small volume by module design, then an explosion with the formation of debris with very high kinetic energy may occur resulting in substantial structural damage to the converter and surrounding elements. Serious injuries to exposed personnel cannot be excluded.

The design rules for minimizing explosion hazards are known. The package has to be designed such that the plasma can expand freely in a defined direction and that no massive parts are obstructing the expansion. An example is ABB's FLIP® module which generically consists of a low inductance strip line with windows for ceramic substrates. Each substrate carries four chips. The windows are filled with gel and covered by a thin rubber foil. It is found that the prime parameter controlling the explosion damage is the released energy. Up to a released energy of about 15 kJ no high velocity ejection of material occurs. At 20 kJ fragments of gel and of the rubber cover are ejected and the module structure breaks up. The important point is that no massive metallic parts are ejected and thus there is no danger of major consecutive damage.

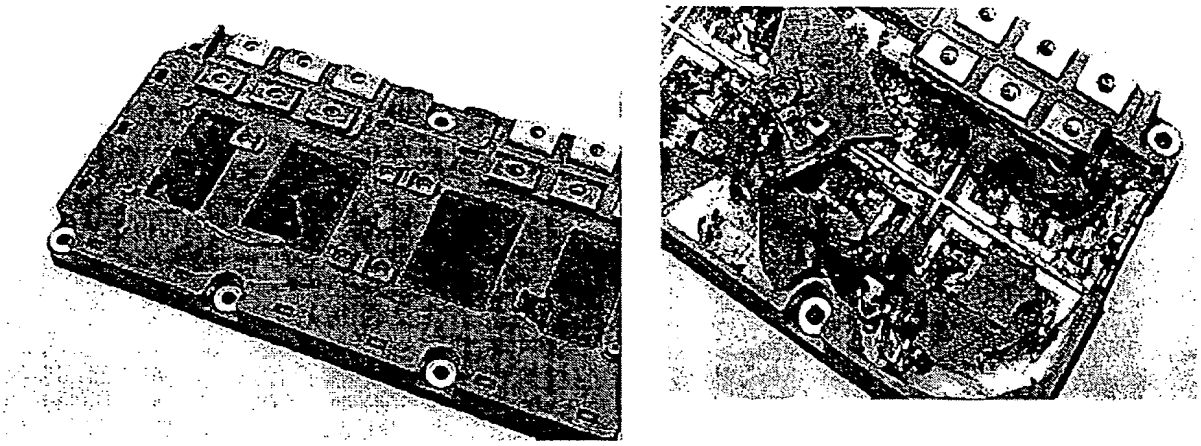

Fig 4 a (left) shows the result of an explosion test with a discharged energy of 7.2 kJ. The module structure is damaged but no parts are ejected. At 20.3 kJ (Fig. 4 b, right) fragments of plastic and gel are ejected but the massive, metallic parts are still in place.

Power and temperature cycling reliability is still an issue for traction applications. The substrate - ground plate interface seems to determine the limiting ΔT at a given wear out lifetime. This has lead to the search for materials with a better match of thermal expansion coefficients. AlSiC is considered a prime candidate as ground plate material. AlSiC is a metal matrix compound formed by first baking SiC powder at a temperature substantially below the sintering temperature such that mechanical integrity is obtained but that the open porosity is conserved [7]. The material is then infiltrated with Al and forms a compound with basically metallic electrical and thermal conductivity but a thermal expansion coefficient close to a ceramic.

First data indicate that AlSiC virtually eliminates the substrate - ground plate power cycling problem for Al_2O_3 substrates and improves the solder reliability for AlN substrates. However, the problem is simply shifted to the next weak spot which is the substrate - die solder interface. The net gain in cycles to wear out at a given ΔT is estimated to be about a factor 4. This estimate is not very solid, more data are needed. The interface AlSiC to metallic cooler needs a particular attention because of its large thermomechanical mismatch. Direct water cooling is an elegant solution which avoids the ground plate - cooler interface and its associated problems.

For industrial motor drives and for railway systems with a 3 kV DC line, 6.5 kV modules with 3 - 3.5 kV DC capability would be a very attractive solution. One of the obstacles from the packaging side for high voltage modules (4.5 kV, 6.5 kV) are the international standards for partial discharge (PD) inception and extinction voltages. From a reliability point of view the requirement is that no partial discharges occur at operating conditions. For partial discharges it is mostly the AC component which counts. A reasonable test condition to ensure long term reliability would be to test at a voltage which is nominal DC plus twice nominal AC. Present standards ask for much higher test voltages which can be met only by unreasonably large and expensive packages. 4.5 kV modules are available from more than one supplier and 6.5 kV chips are in a test phase.

4. Improving high voltage IGBT's by plasma engineering

In many discussions on the pros and cons of different device concepts it is forgotten, that the performance of a given device does not depend on its acronym but on its plasma distribution. The plasma distribution which gives optimum overall losses in a switch is basically identical for all high voltage switching devices.

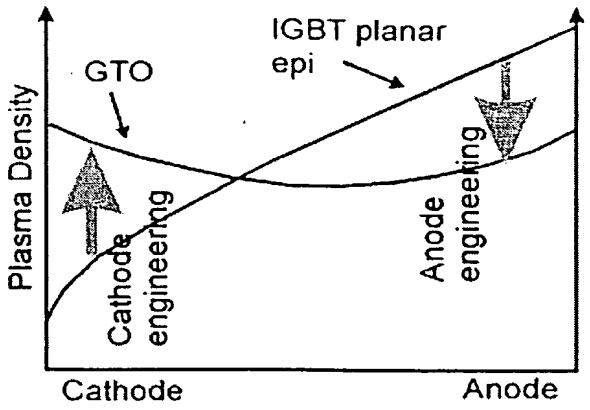

Fig. 5 Plasma distribution in a GTO and an epi IGBT. The design goal for modern IGBT's is to achieve a more symmetrical plasma distribution by emitter engineering.

The optimum plasma distribution between anode and cathode is close to a symmetric catenary. Latching devices such as the GTO or GCT have injecting emitters on both sides. This make a relatively symmetric plasma distribution easy to achieve. The two end points of the plasma distribution are defined by the respective emitter efficiencies, the depression in the center by recombination.

For GTO's and GCT's the optimum involves having a high efficiency cathode and a low efficiency anode emitter. The tools to reduce anode emitter efficiency are: n+ anode shorts, transparent emitter, heavy particle irradiation. For low-loss buffer-layer structures anode shorts lead to high trigger currents. Transparent emitters are thus the design tool of choice. Today's state of the art GTO's and GCT's are very close to the optimum.

The standard epi IGBT has two major drawbacks with respect to plasma engineering. First, and this applies to all IGBT's, minority carrier injection occurs only at the anode. The plasma distribution has thus a strong tendency to peak at the anode and to decrease towards the cathode. The design goal is thus to increase the plasma density at the cathode and to decrease it at the anode in order to reach a nearly symmetrical distribution.

We first consider the anode side. Anode engineering in an epi IGBT is close to impossible, because the anode is not easily accessible from the back side. The current trend to bulk (NPT) IGBT's is primarily driven by the high cost of thick epi layers. However, bulk IGBT's allow also performance improvements due to anode engineering. Currently bulk IGBT's are manufactured by processing a wafer with minimum thickness compatible with high yield. At the end of the process the wafer is thinned and the anode metallisation is applied. A low efficiency anode is formed by tempering the anode metal. Further adjustments by particle irradiation are possible, because the anode is accessible. Present processing technology does not allow to reduce the thickness to the optimal thickness of bulk IGBT's in terms of losses for blocking voltages of 1200 V and less. Further improvements can be expected.

In the volume of the device the plasma density can be adjusted by recombination centers. Traditionally this was accomplished by diffusing noble metal ions. This process is difficult to control. Particle irradiation leads to a much better process control. Electrons provide a nearly homogeneous distribution of recombination centers. With protons or He ions, arbitrary profiles of recombination centers can be generated which allows a much more precise plasma engineering.

We now address the cathode side. The IGBT has no injecting emitter at the cathode. Without special measures the plasma density thus decreases from anode to cathode. Two design tools are available to improve the situation. The first is to increase the inflow of electrons from the MOS channels and the second is to restrict the outflow of holes at the cathode. Increasing the inflow of electrons is accomplished by increasing the packaging density of MOS channels. This requires the reduction of feature size and/or trench structures. For geometrical reasons, trench structures also form obstacles to the outflow of holes.

In most trench structures the restricted outflow of holes leads to an overcompensation of the dip at the cathode. The density has now a peak at the cathode and steadily falls towards the anode. The result is a high desaturation current which makes short circuit protection impossible. Recently trench designs have been announced which achieve a more symmetrical plasma density and which provide short circuit SOA.

It is also possible to increase the plasma density at the cathode without increasing electron injection efficiency by increasing the stripe pitch in planar IGBT designs. This leads to very favorable Vt(Eoff) curves and simple, low-cost technology, but also to a tendency of slow turn on and thus high Eon. The ratio of desaturation to nominal current is very small in this design and excellent short circuit robustness is achieved.

A third option is to create a barrier for the out flow of holes in the form of an n-layer in front of the p-well [8]. This gives acceptable desaturation current and short-circuit behavior. The n-layer, however, leads to high field peaks at the cathode which may substantially reduce cosmic-ray robustness.

In order to achieve an optimal plasma distribution, a trench structure is not a must. The same can be achieved with simpler technologies. The main advantage of the trench structure in the 1200 V range and below is the avoidance of the so called JFET voltage drop [9] which is approximately 0.5 V for a typical planar 1200 V IGBT.

The general statement thus is that for a 1200 V trench IGBT the $E_{off}(V_t)$ technology curve is shifted by approximately 0.5 V compared to an optimized planar structure. Since the bulk design is inherently more robust than an epi structure, short-circuit stability seems to be feasible in future, optimized structures. Paralleling of trench devices is still an issue due to the negative temperature coefficient and due to the very high transconductance.

The 0.5 V performance advantage of the trench IGBT is counteracted by a cost disadvantage due to process complexity and yield. As the technology matures, the disadvantage will decrease and the trench design will gain market share. For higher voltages the performance gain of the trench structure with respect to other forms of plasma engineered devices is less clear.

Even less clear is the fate of alternate device structures which form mostly the subject of university studies. Since proper plasma engineering leads to plasma distributions in IGBT's which are very close to those of latching devices, the expected performance gain of any novel device structure with respect to the IGBT is relatively small.

5. Diodes

In snubberless circuits without voltage clamp the performance limiting element is in most cases the freewheel diode. Plasma engineering of the diode follows the same principles as for IGBT's and GTO's: In practice this means reduction of plasma density at the anode. The method of choice is irradiation with heavy particles such as protons or alpha's. Lifetime engineering by noble metals also gives excellent properties but is very hard to control compared to heavy particle irradiation. Diode optimization is arguably the ultimate challenge for the device design engineer.

In the 1200 V range the same trend as for IGBT's is evident. Epitaxial structures are no longer competitive for cost reasons. Bulk pin diodes cannot be thinned similar to IGBT's because the junction termination cannot be applied before the thinning. A promising route is to start with a wafer of the minimum processable thickness and to reduce the n-base thickness by deep diffusion. Plasma engineering by heavy particles has been very successful but has not reached full maturity yet.

The turn on losses in a switch with its freewheeling diode can be split into a circuit dependent part E_{on}^{c} and a device dependent part E_{on}^{d}. Subject to some simplifying assumptions E_{on}^{c} is given by:

$$E_{on}^{c} = \frac{I_{load} \cdot V_{dc}}{2} \cdot \tau \cdot (1 + \frac{I_{rr}}{I_{load}})^2$$

$$\tau = I_{load} \cdot (\frac{dI}{dt})^{-1}$$

Further analysis shows that minimum losses are achieved, if τ is chosen such that $I_{rr} \approx I_{load}$. The potential for further improvement of Si based high voltage diodes is limited. No order of magnitude improvements can be expected.
SiC diodes allow a reduction of the circuit specific turn-on losses by at least an order of magnitude. The design of hybrid modules with silicon IGBT's and SiC diodes is thus a very attractive option.

SiC based Schottky and JBS diodes have been built and tested for blocking voltages up to 2000 V and pin diodes up to 5 kV. The limiting factor for high power applications is the defect density of SiC wafers. It seems feasible to have prototypes of modules with SiC diodes with ratings of several 100 A before the end of the century. In order to be cost effective, the diodes have to be operated at very high current densities. This results in a high device temperature. The operation of SiC diodes at temperatures in excess of 400 °C is unproblematic. However, there are no known packaging technologies which would withstand a high number of power cycles at temperature intervals of > 200 °C.

6. Summary

	Trend	Driver	Barrier
IGBT (chip)	Trench	Loss reduction	Cost, short circuit protection, paralleling
	Higher voltage	System cost reduction	Losses, insulation, diode performance
	Higher frequency	System cost reduction	Losses, device cost, EMI
IGBT (package)	MMC baseplate (e.g. AlSiC)	Higher allowed ΔT, higher wear-out lifetime	Poor CTE matching to cooler, brittle
	Higher voltage	System cost reduction	Insulation and partial discharge standards
	Standardization	Cost reduction	Conflict with integration
	Integration	System cost reduction	Conflict with standardization
	Higher power/thermal cycling capability	Higher allowed ΔT, lower cost	Needs improved interface and integration technologies
	Higher volume power density	cost and volume reduction	Power cycling reliability
	Direct water cooling	Improved W/°K, no interface baseplate - cooler	Market acceptance
	SiC freewheel diodes	Frequency up, losses down	Defect density SiC, cost, packaging reliability
GCT, IGCT	Higher voltage	System cost	Passivation
	Monolithic diode	Cost	Requires n-buffer GTO
	Lower back porch current	Gate unit power and cost	
	Non hermetic package	Cost	Passivation
	Higher current	System cost	Stray inductance
	High voltage, medium/small current	System cost, low cost package/gate unit	Passivation
Diode	Higher dI/dt	Losses, frequency	Diode SOA
	Heavy particle lifetime profiling	dI/dt, reverse recovery	Cost, logistics
GTO	Loss of market share to IGBT and GCT	Cost, performance	
Thyristor	Monolithic antiparallel thyristor (BCT)	Cost	Current 2x smaller

Tab. 3: Trends in high power electronic devices

Tab. 3 shows the trends in active part and packaging of high power devices. Most issues are interdisciplinary. No longer can the semiconductor specialist base his development on a back of the envelope spec, the packaging engineer ignore state of the art materials science and the converter designer treat the device as a black box.

Acknowledgments

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